ABSTRACT OF THE DISCLOSURE

An oversampling modulator device includes an adder outputting an signal indicating a sum of an input signal and a first delayed signal, the input signal having a plurality of bits, the output signal having upper bits included in a first signal and the remaining bits included in a second signal. A subtractor outputs a signal indicating a difference between the first signal and a second delayed signal. A first delay unit outputs the first delayed signal by delaying a third signal having upper bits produced by the subtraction signal and lower bits produced by the second signal. A quantizer performs quantization processing of the third signal and outputs a quantization signal having a predetermined number of bits. A second delay unit outputs the second delayed signal by delaying the quantization signal. The quantizer selects specific bits included in the third signal to generate the quantization signal.